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EXAMINER	
BONZO, BRYCE P	
ART UNIT	**PAPER NUMBER**
2114	

DATE MAILED: 11/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/886,959	AVIZIENIS, ALGIRDAS	
	Examiner	Art Unit	
	Bryce P Bonzo	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-66* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-49 and 52-66* is/are rejected.

7)☒ Claim(s) *50 and 51* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

NON-FINAL OFFICIAL ACTION

Status of the Claims

Claims 1-13, 19, 24, 27, 32-41, 54, 61, 64, 65 are rejected under 35 USC §112, second paragraph.

Claims 4, 16, 26, 36, 47, 59, 63 and 66 are rejected under 35 USC §112, fourth paragraph.

Claims 48 is rejected being a duplicate of claim 43.

Claims 13-15, 17, 18, 20-23, 28-31, 42-46, 48, 49, 52, 53, 55-58, 60 and 62 are rejected under 35 USC §102.

Non-Considered Document

The newly submitted IDS does not provide item 1. As such the Examiner is unable to consider the document. The PTO-1449 has been struck at line 1 accordingly. All other documents have been considered and initialed. A copy of the submitted PTO 1449 has been attached.

Duplicate Claim Objection

Claim 48 is objected to under 37 CFR 1.75 as being a substantial duplicate of claim 43. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is

proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Rejections under 35 USC §112, second paragraph

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-13, 19, 24, 27, 32-41, 54, 61, 64, 65 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claims 1-13, the Examiner is unable to determine the bounds of "exclusively hardware...having substantially no software". An exclusively hardware element will not have any software. By using the word substantially, the Examiner is confused as to whether or not an given element is permitted to have a software component when attempting to meet the limitations of the claim. How much software is permitted in a hardware element, which should not even have software? The Examiner is unable to determine with any degree of certainty how much software in an element is permissible. For example: Is an element which carries out the claim functioned but contains software programming not relevant to the claimed function substantially free of software? If an element which carries out the functions recited in the claims, and hardened software is used to aid in the function, is the element substantially free of software? What degree

of functionality must be implemented in software before the element is no longer substantially free of software?

As per claims 2, 3, 7, 12, 19, 24, 27, 32-41, 54, 61, 64 and 65, the Examiner is unable to determine the bounds of "substantially exclusively made up of substantially commercial, off-the-shelf components." The Examiner is unable to determine a reasonable limit to the claims. For example, is a stock commercially available processor which has been over clocked 1% substantially off-the-shelf? What if the same processor has over clocked by 20%, is the resulting processor still off-the-shelf? What a user modifies a product against the manufacturer's wishes, as disabling the frequency clocking protections and over clocking a processor? At what point does the increased possibility of failure due to modification render a device no longer substantially exclusively commercially, off-the-shelf? Is the degree of commercial, of-the-shelf determined by the amount of effort, time or money used to modify element? At what point does the effort, time or money render an element no longer substantially commercial or off-the-shelf.

Rejections under 35 USC §112, fourth paragraph

The following is a quotation of the fourth paragraph of 35 U.S.C. 112:

> Subject to the following paragraph, a claim in dependent form shall contain a reference to a claim previously set forth and then specify a further limitation of the subject matter claimed. A claim in dependent form shall be construed to incorporate by reference all the limitations of the claim to which it refers.

Claims 4, 16, 26, 36, 47, 59, 63 and 66 are rejected under 35 USC §112, fourth paragraph as they fail to further limit the scope of the claims. The *such computer system* of these claims is each case has already been claimed verbatim in the parent claim. These claims recite a "such computer." Each claim depends from a parent claim containing in the preamble: "failure of a computer system." Each parent claim then recites the failure in the body of the claim. As the failure is recited in the body of the claim, the descriptors from the preamble breath life into the bodily recited limitation and warrant patentable weight. As the Examiner is then required to find the computer system, reciting "such computer system" in its own claim becomes a redundant limitation, and when presented singularly fails to meet eh requirements of §112, fourth paragraph, namely that a dependant claim must further limit the parent.

Rejections under 35 USC §102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 13-15, 17, 18, 20-23, 28-31, 42-46, 48, 49, 52, 53, 55-58, 60 and 62 are rejected under 35 U.S.C. 102(e) as being anticipated by Rasmussen (United States Patent No. 6,754,846 B2).

As per the claims, Rasmussen discloses:

13. Apparatus for deterring failure of a computing system; said apparatus comprising:

a network of components having terminals for connection to such system (column 2, lines 14-22); and

circuits of the network for operating programs to guard such system from failure (column 2, lines 55-60);

the circuits comprising portions for identifying failure of any of the circuits and correcting for the identified failure (column 2, lines 55-60).

14. The apparatus of claim 13, wherein: the program-operating portions comprise a section that corrects for the identified failure by taking a failed circuit out of operation (column 2, lines 5-14).

15. The apparatus of claim 14, wherein: the program-operating portions comprise a section that substitutes and powers up a spare circuit for a circuit taken out of operation (column 3, lines 51-56).

17. The apparatus of claim 13, wherein:

the program-operating portions comprise at least three of the circuits (column 2, line 1); and

failure is identified at least in part by majority vote among the at least three circuits (column 2, lines 55-60).

18. The apparatus of claim 13, particularly for use with a computing system that has at least one software subsystem for conferring resistance to failure of the system(column 7, lines 63 through column 8, lines 6); and wherein:

the circuits comprise substantially no portion that interferes with such failure-resistance software subsystem (no such interference is disclosed, and such interference would be contrary to the intent of the disclosure).

20. The apparatus of claim 13, particularly for use with a computing system that has plural generally parallel computing channels (column 2, lines 1-4); and wherein:

the circuits comprise portions for comparing computational results from such parallel channels (column 2, lines 5-8).

21. The apparatus of claim 20, wherein: the parallel channels of the computing system are of diverse design or origin (column 2, lines 1-13 as the channels originate from different sources, they are independent of origin).

22. The apparatus of claim 13, particularly for use with a computing system that has plural processors (column 2, lines 17-22); and wherein:

the circuits comprise portions for identifying failure of any of such processors and correcting for identified failure (column 2, lines 55-61).

23. The apparatus of claim 13, wherein: the circuits comprise modules for collecting and responding to data received from at least one of the terminals, said modules comprising (column 2, lines 16-17):

at least three data-collecting and -responding modules (column 2, lines 16-17), and

processing sections for conferring among the modules to determine whether any of the modules has failed (column 2, lines 55-60).

25. Apparatus for deterring failure of a computing system that has at least one software subsystem for conferring resistance to failure of the system; said apparatus comprising:

a network of components having terminals for connection to such system (column 2, lines 14-22); and

circuits of the network for operating programs to guard such system from failure (column 2, lines 55-60);

the circuits comprising substantially no portion that interferes with such failure-resistance software subsystem (no such interference is disclosed, and such interference would be contrary to the intent of the disclosure).

26. The apparatus of claim 25, further comprising: such computing system, including such at least one software subsystem (column 2, lines 4-5).

28. The apparatus of claim 25, particularly for use with a computing system that has plural generally parallel computing channels; and wherein (column 2, lines 1-4): the circuits comprise portions for comparing computational results from such parallel channels (column 2, lines 5-8).

29. The apparatus of claim 28, wherein: the parallel channels of the computing system are of diverse design or origin (column 2, lines 1-13 as the channels originate from different sources, they are independent of origin).

30. The apparatus of claim 25, particularly for use with a computing system that has plural processors (column 2, lines 14-22); and wherein:

the circuits comprise portions for identifying failure of any of such processors and correcting for identified failure (column 2, lines 55-61).

31. The apparatus of claim 25, wherein: the circuits comprise modules for collecting and responding to data received from at least one of the terminals, said modules comprising (column 2, lines 16-17):

at least three data-collecting and -responding modules (column 2, lines 16-17)), and

processing sections for conferring among the modules to determine whether any of the modules has failed (column 2, lines 55-60).

42. Apparatus for deterring failure of a computing system that is distinct from the apparatus and that has plural generally parallel computing channels; said apparatus comprising: a network of components having terminals for connection to such system (column 2, lines 55-60); and circuits of the network for operating programs to guard such system from failure (column 2, lines 55-60); the circuits comprising portions for comparing computational results from such parallel channels (column 2, lines 55-60).

43. The apparatus of claim 42, wherein: the parallel channels of the computing system are of diverse design or origin (column 2, lines 1-13 as the channels originate from different sources, they are independent of origin).

44. The apparatus of claim 42, wherein: the comparing portions comprise at least one section for analyzing discrepancies between the results from such parallel channels (column 2, lines 55-60).

45. The apparatus of claim 44, wherein: the comparing portions further comprise at least one section for imposing corrective action on such system in view of the analyzed discrepancies(column 2, lines 55-60).

46. The apparatus of claim 45, wherein: the at least one discrepancy-analyzing section uses a majority voting criterion for resolving discrepancies (column 2, lines 55-60).

48. The apparatus of claim 47, wherein: the parallel channels of the computing system are of diverse design or origin (column 2, lines 1-13 as the channels originate from different sources, they are independent of origin).

49. The apparatus of claim 48, wherein

the comparing portions comprises circuitry for performing an algorithm to validate a match that is inexact (column 2, lines 5-8: the analog case)

52. The apparatus of claim 42, particularly for use with a computing system that has plural processors (column 2, lines 4-6; and wherein:

the circuits comprise portions for identifying failure of any of such processors and correcting for identified failure (column 2, lines 23-37).

53. The apparatus of claim 42, wherein: the circuits comprise modules for collecting and responding to data received from at least one of the terminals, said modules comprising (column 2, lines 16-17):

at least three data-collecting and -responding modules (column 2, lines 16-17), and

processing sections for conferring among the modules to determine whether any of the modules has failed (column 2, lines 5-60).

55. Apparatus for deterring failure of a computing system that has plural processors; said apparatus comprising:

a network of components having terminals for connection to such system (column 2, lines 14-22); and

circuits of the network for operating programs to guard such system from failure(column 2, lines 55-60);

the circuits comprising portions for identifying failure of any of such processors and correcting for identified failure (column 2, lines 55-60).

56. The apparatus of claim 55, wherein: the identifying portions comprise a section that corrects for the identified failure by taking a failed processor out of operation (column 2, lines 5-14

57. The apparatus of claim 56, wherein: the section comprises parts for taking a processor out of operation only in case of signals indicating that the processor has failed permanently (all failures in the system of Rasmussen are permanent such is the degree of fault tolerance demanded).

58. The apparatus of claim 55, wherein: the identifying portions comprise a section that substitutes and powers up a spare circuit for a processor taken out of operation (column 2, lines 24-27).

60. The apparatus of claim 55, wherein: the circuits comprise modules for collecting and responding to data received from at least one of the terminals, said modules comprising (column 2, lines 16-17):

at least three data-collecting and -responding modules (column 2, lines 16-17), and

processing sections for conferring among the modules to determine whether any of the modules has failed (column 2, lines 16-17).

62. Apparatus for deterring failure of a computing system; said apparatus comprising:

a network of components having terminals for connection to such system (column 2, lines 14-22); and

circuits of the network for operating programs to guard such system from failure (column 2, lines 55-60);

the circuits comprising modules for collecting and responding to data received from at least one of the terminals (column 2, lines 55-60), said modules comprising:

at least three data-collecting and -responding modules (column 2, lines 16-17), and

processing sections for conferring among the modules to determine whether any of the modules has failed (column 2, lines 16-17).

Allowable Matter

Claims 50 and 51 remain objected to while containing allowable subject matter as set forth in the previous Official Action.

Applicant is reminded the claims are indicated as allowable as a whole including any intervening base claims.

Response to Applicant's Arguments

I. The Examiner has rewritten the rejections under 35 USC §112, second paragraph to more clearly illustrate why the Examiner is unable to determine a scope for the claims. If this rational is insufficient to sway the Applicant to remove the language, an appeal to the Board of Patent Appeals and Interferences recommended.

II. The status of the IDS is stated above.

III. The Examiner has rewritten the rejections under 35 USC §112, fourth paragraph to more clearly illustrate why the Examiner is unable to determine a scope for the claims. If this rational is insufficient to sway the Applicant to remove the language, an appeal to the Board of Patent Appeals and Interferences recommended.

IV. The previous rejection under 35 USC §102(b) has been vacated, as the Examiner admits to transposing the dates of publication. As such this action has not been made final, while presenting a new rejection under 35 USC §102(e). The effective filing date of Rasmussen is December 18th, 1998. As the rejection is entirely new, the Examiner is unable to anticipate any short comings in the reference the Applicant may find.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bryce P Bonzo whose telephone number is (571)272-3655. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571)272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Bryce P. Bonzo

Bryce P Bonzo
Examiner
Art Unit 2114